IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/640,988	Confirmation No. 9195
Applicant	:	LUECK, Andrew W.	
Filed	:	08/14/2003	
TC/A.U	:	2112	
Examiner	:	Huynh, Kim T.	
Docket No.	:	TI-35560	
Customer No.	:	23494	
For	:	PCI EXPRESS TO PCI TRANSLATION BRIDGE	

AMENDMENT UNDER 37 C. F. R. § 1.116

Assistant Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the official action mailed April 18, 2006, Applicant respectfully submits the following amendments and remarks in connection with the above identified application.

Amendments to the Claims begin on Page 2 of this paper.

Remarks begin on Page 7 of this paper.

Amendments to the Claims

1. (Previously Presented) A PCI to a serial switched topology used to connect peripheral devices to a computer bridge comprising:

a PCI interface couplable to a PCI bus having PCI compatible devices connected thereto;

a port arbitration circuit for controlling grant and stop lines of the PCI compatible devices to force time – based arbitration on the PCI devices connected to a PCI bus to guarantee bandwidth to upstream data sent from a predetermined one of the PCI compatible devices and for allocating the data to a predetermined one of a plurality of virtual cannels supported by a serial switched topology used to connect peripheral devices to a computer,

a virtual channel arbitration circuit for allocating the virtual channels to an output port of the bridge; and

the serial switched topology interface coupled between the virtual channel arbitration circuit and the output port.

2. (Original) The bridge of Claim 1 further comprising a port arbitration table coupled to the port arbitration circuit, the port arbitration circuit, the port arbitration table determining PCI bus transactions to guarantee isochronism of data transfers.

3. (Original) The bridge of Claim 2 further comprising a bus traffic management circuit responsive to the control data stored in the port arbitration table for controlling the port arbitration circuit.

4. (Original) The bridge of Claim 1 further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to the PCI bus.

5. (Original) The bridge of Claim 3 further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to the PCI bus.

6. (Original) The bridge of Claim 5 wherein the PCI bus arbiter grants control of the PCI bus to a PCI compatible device connected to the bus, the PCI bus arbiter being controlled by the bus traffic management circuit to grant control of the PCI bus to a PCI compatible device sending isochronous data at predetermined intervals to maintain the isochronism of the data.

7. (Original) The bridge of Claim 1 further comprising an upstream virtual channel window control register, the register being addressed by a PCI compatible device for sending isochronous data.

8. (Previously Presented) The bridge of Claim 7 wherein the window control register is located within the serial switched topology configuration space.

9. (Original) The bridge of Claim 7 wherein the window control register is located within extended PCI configuration space.

10. (Original) The bridge of Claim 7 wherein the window control register is located in memory.

11. (Original) The bridge of Claim 10 wherein the memory is located within the bridge.

12. (Original) The bridge of Claim 11 wherein the memory is located in memory mapped configuration space.

13. (Original) The bridge of Claim 1 further comprising a virtual channel arbitration circuit.

14. (Original) The bridge of Claim 1 wherein the upstream data is isochronous data.

15. (Original) The bridge of Claim 14 wherein the PCI compatible device is an IEEE 1394 device.

16. (Previously Presented) A method for isochronous transfer of data from a PCI compatible device connected to a PCI bus to a serial switched topology used to connect peripheral devices to a computer comprising:

receiving data at an input port for isochronous transfer from a pre-selected PCI compatible device;

controlling grant and stop lines of PCI compatible devices on the PCI bus to force time-based arbitration on the PCI devices connected to the PCI bus to guarantee bandwidth from the pre-selected PCI device;

allocating the data from the pre-selected device to one of a plurality of virtual channels supported by the serial switched topology;

arbitrating the virtual channels onto an output port.

17. (Original) The method of Claim 16 wherein controlling PCI compatible devices on the PCI bus is in response to control signals generated in response to a port arbitration table.

18. (Previously Presented) The method of Claim 16 further comprising:

writing data from a PCI compatible device to a register defined in a PCI to the serial switched topology bridge to define the data transfer as isochronous.

19. (Cancelled)

20. (Cancelled)

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The examiner has allowed Claims 1-18 and rejects Claims 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by Kelly et al.

Applicants respectfully disagree with the examiner's position and believe that Claims 19 and 20 are distinguished over Kelly for the reason set forth in the response to the previous official action. However, in order to advance the prosecution of this application, Applicant's have cancelled claims 19 and 20 without prejudice in order to place the application in condition for allowance.

Accordingly, Applicants believe that the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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